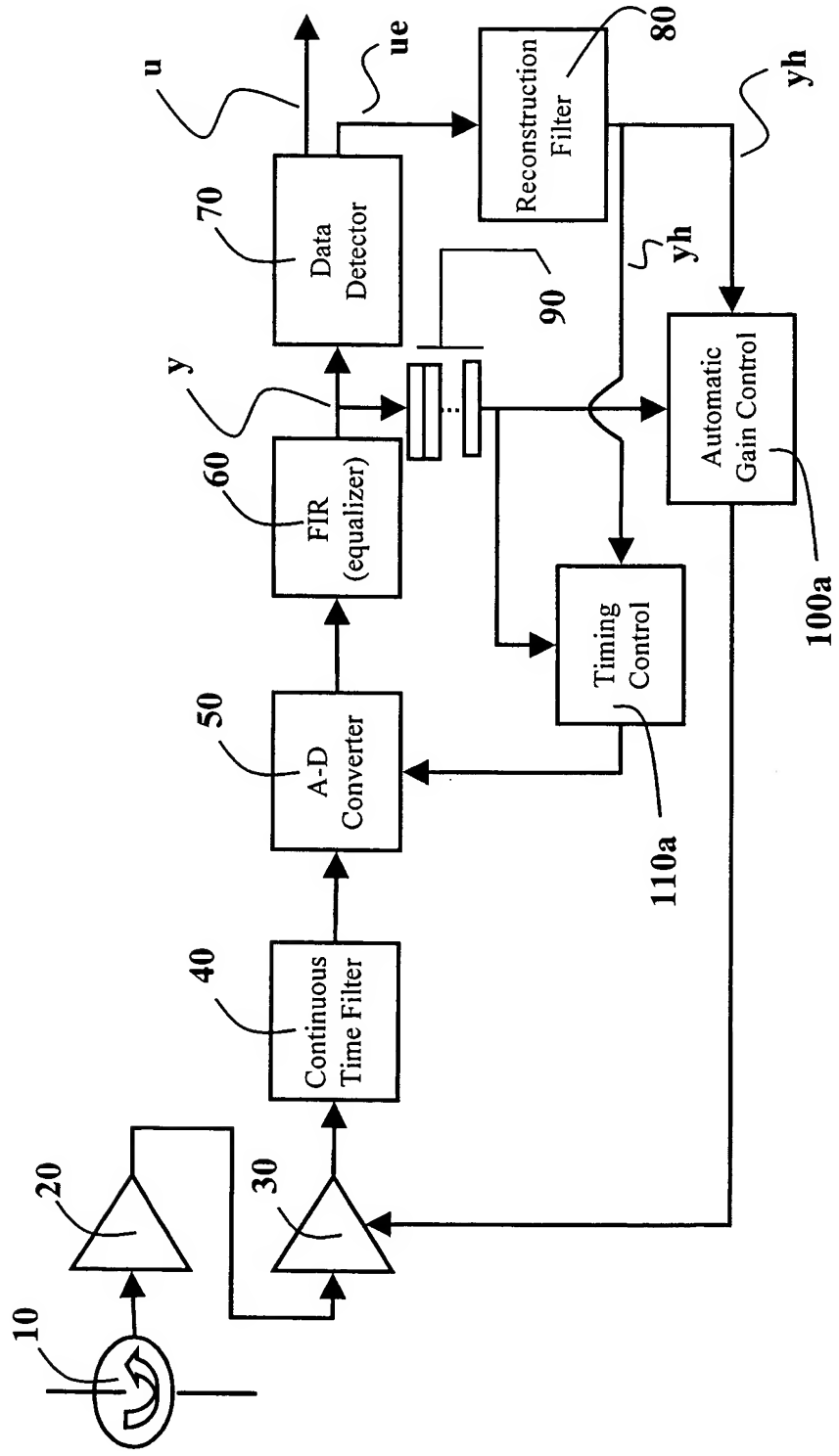


FIGURE 1
Prior Art

FIGURE 2

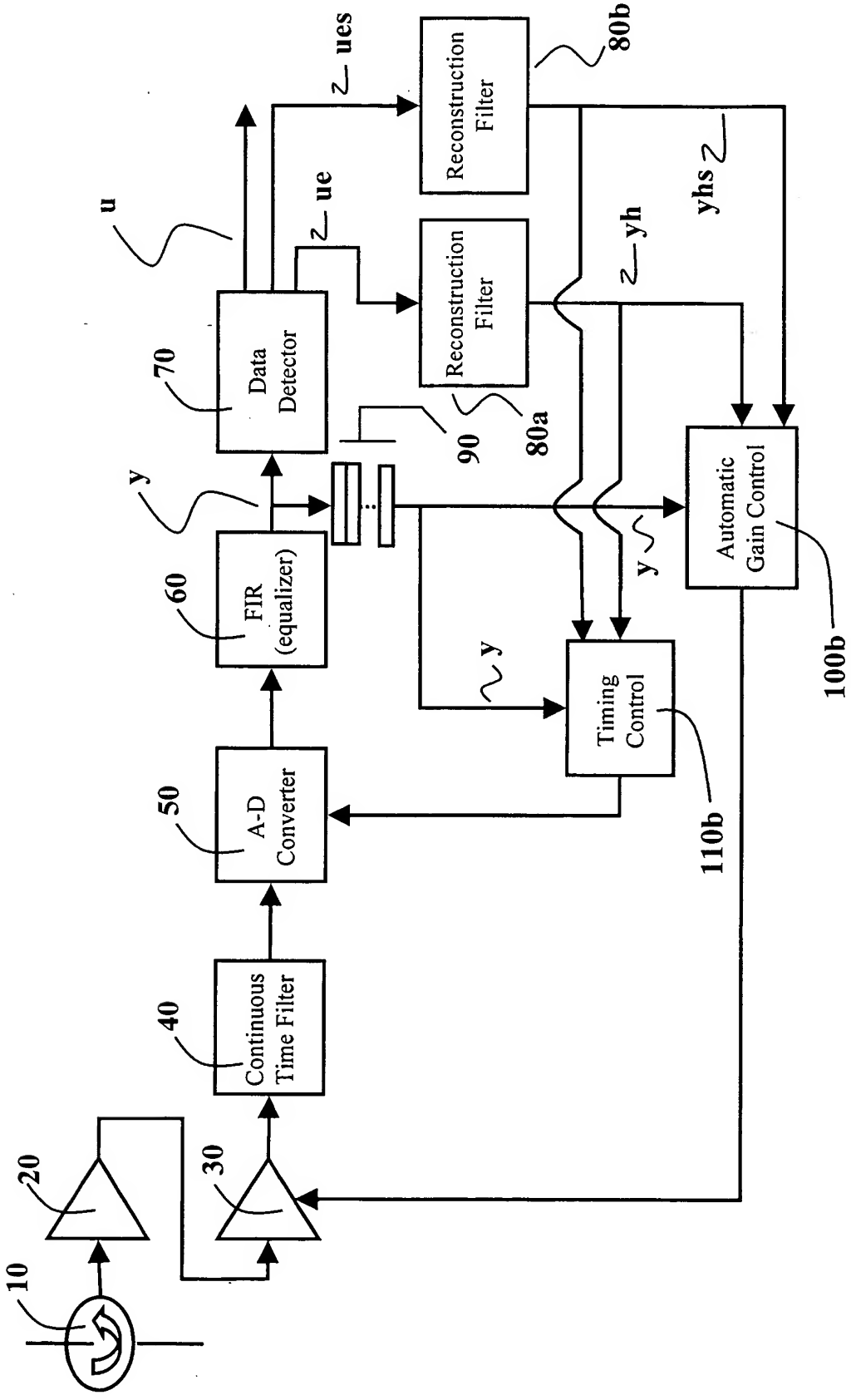

10
20
30
Continuous Time Filter
40
A-D Converter
50
FIR (equalizer)
60
Data Detector
70
u
y
90
Reconstruction Filter
80a
ue
Reconstruction Filter
80b
ues
yh
yhs
Timing Control
110b
Automatic Gain Control
100b

FIGURE 3
Prior Art

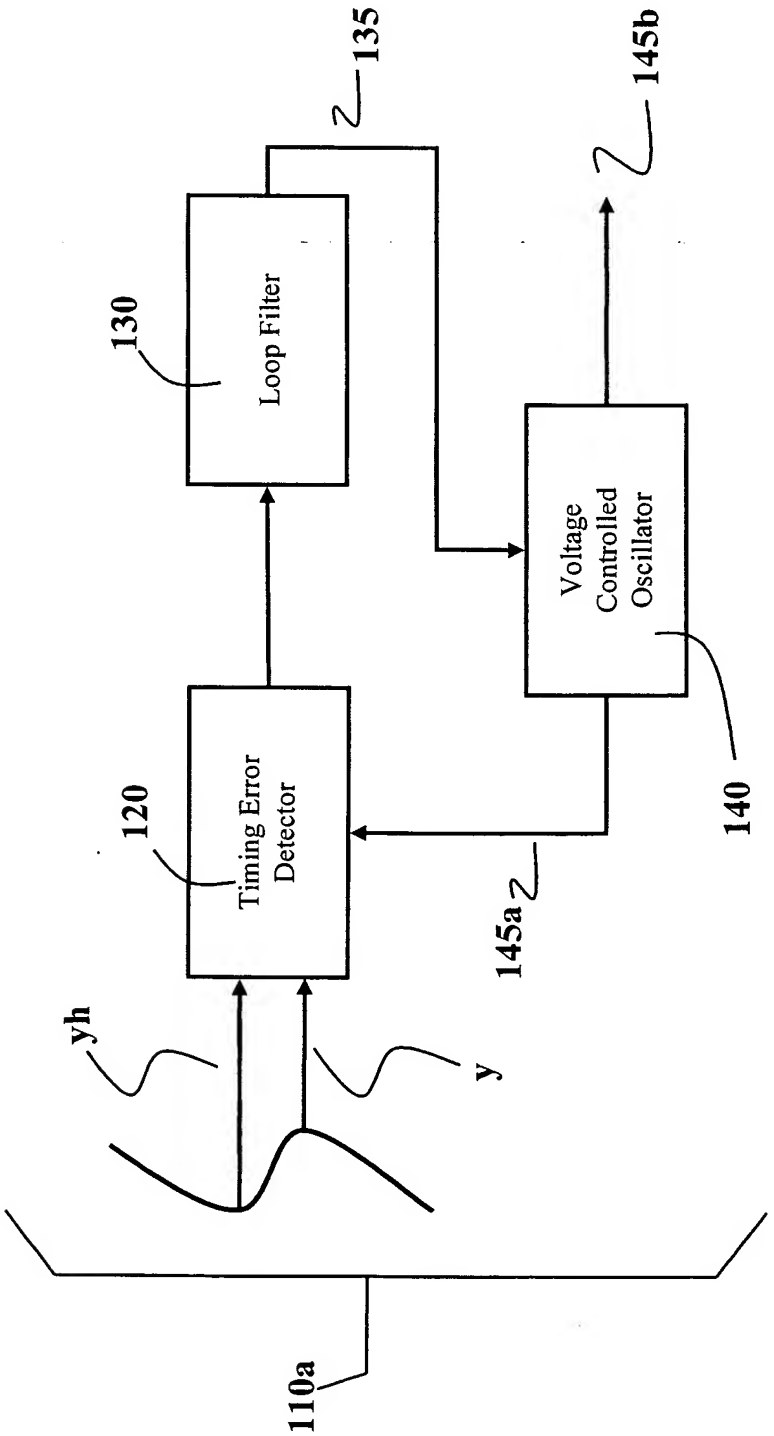


FIGURE 4

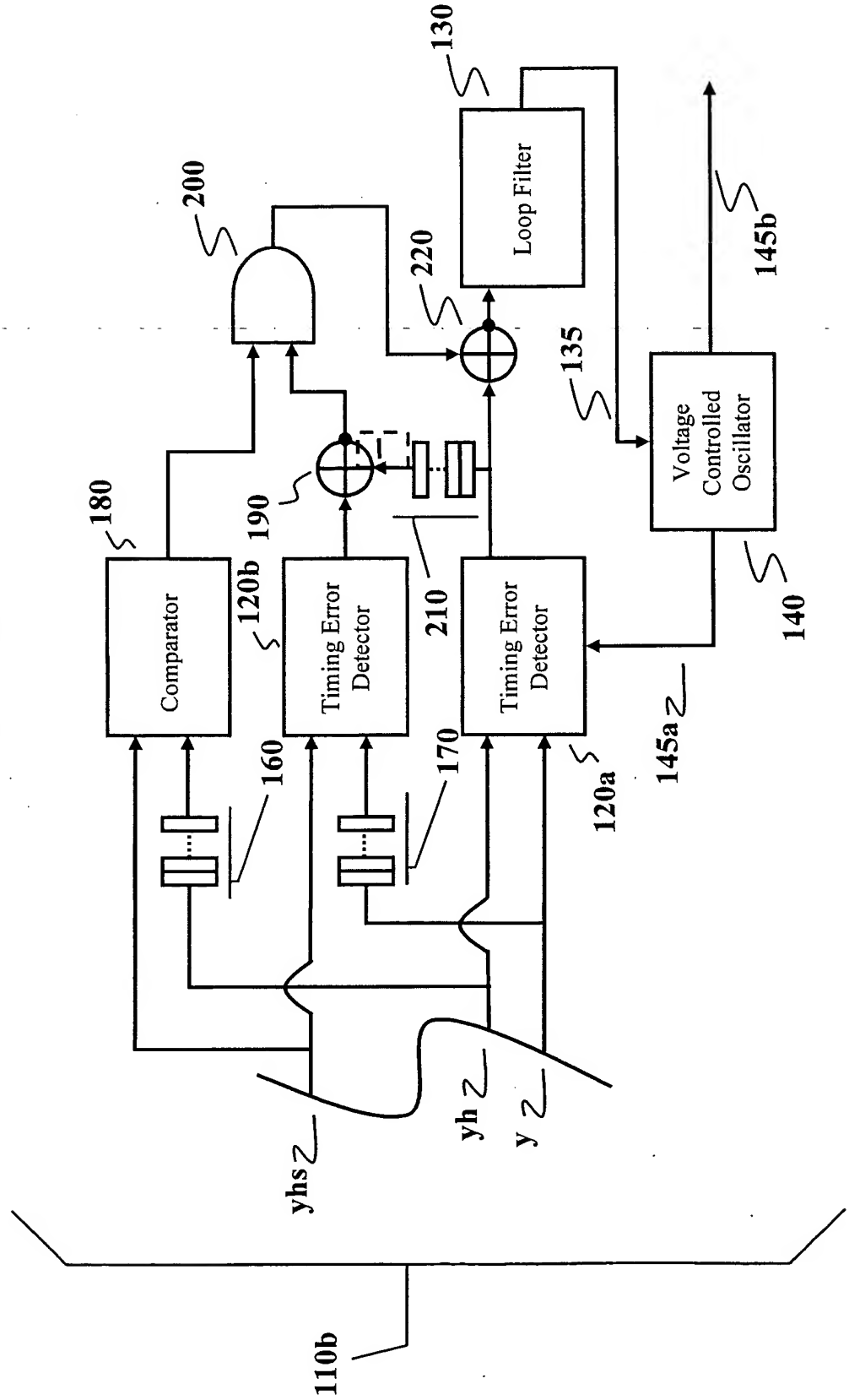

130
Loop Filter
200
220
145b
135
Voltage Controlled Oscillator
180
190
120b
Comparator
Timing Error Detector
210
Timing Error Detector
140
145a
120a
160
170
yhs
yh
y
110b

FIGURE 5

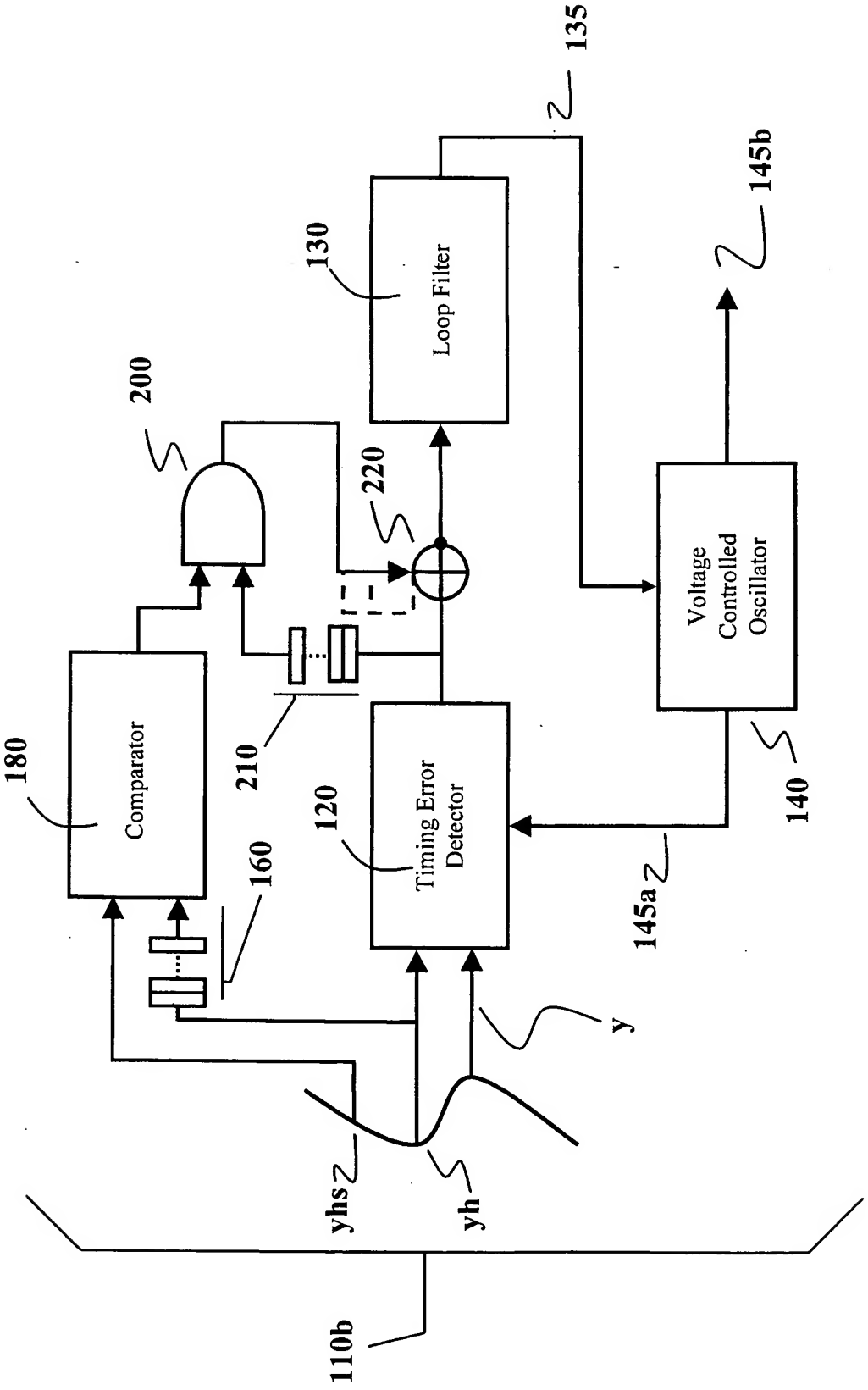

135
145b
130
Loop Filter
200
220
Voltage Controlled Oscillator
180
Comparator
210
120
Timing Error Detector
140
160
145a
y
yhs
yh
110b

FIGURE 6
Prior Art

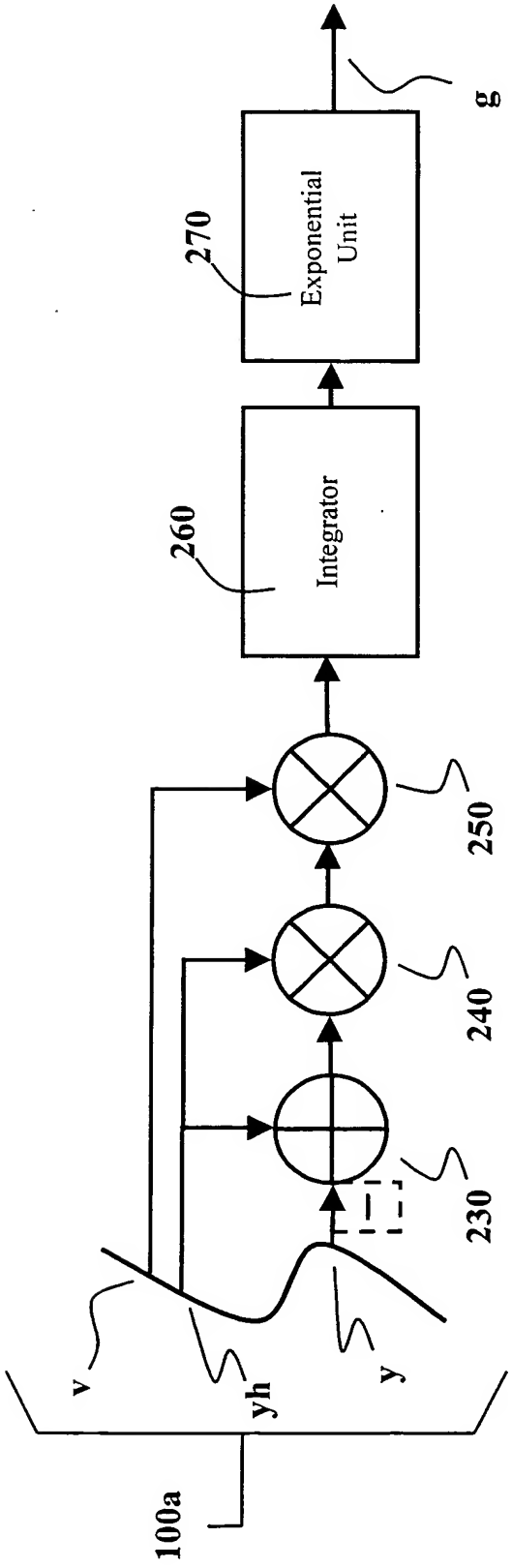


FIGURE 7

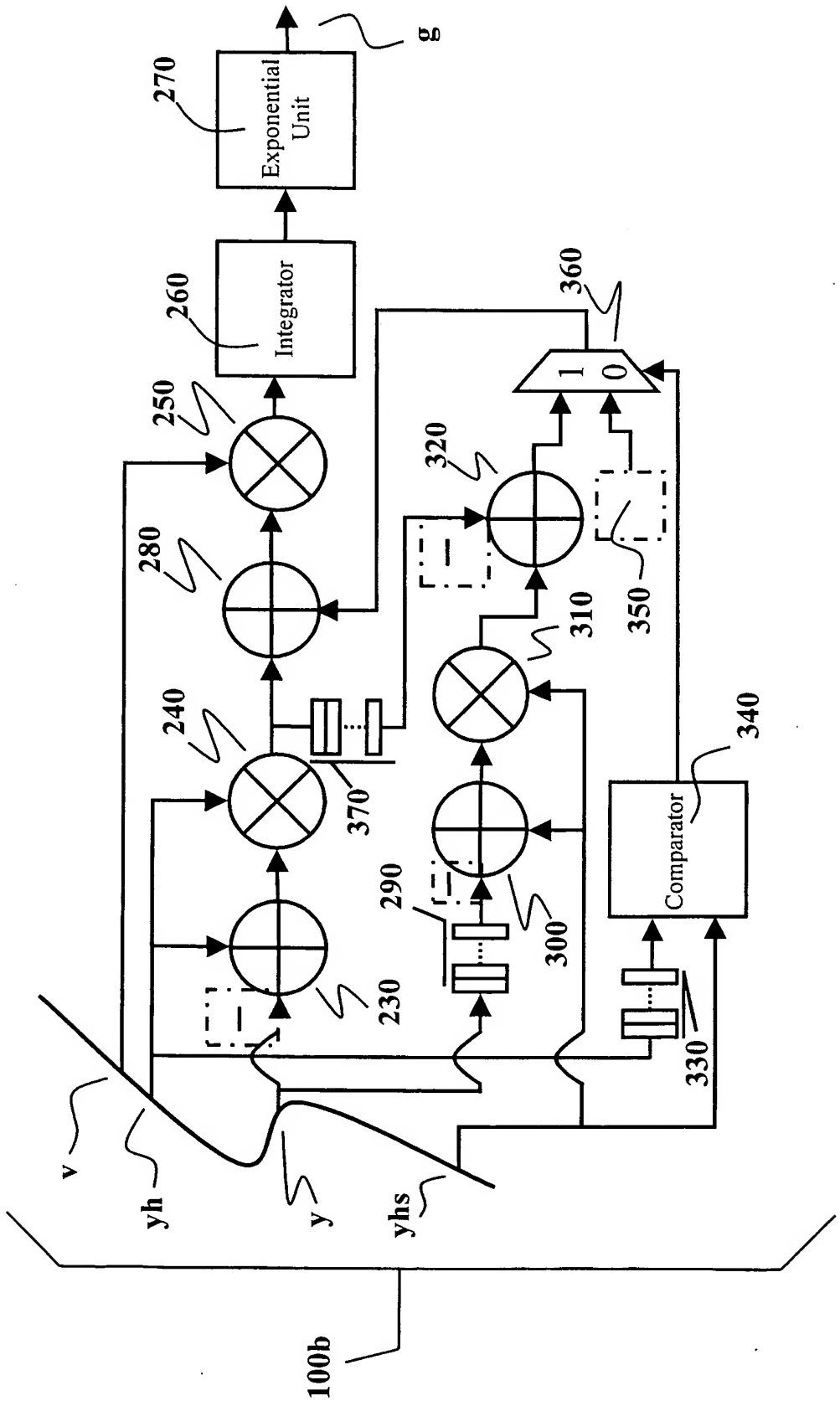

g
270
Exponential Unit
260
Integrator
250
280
240
370
230
290
300
320
310
350
360
1
0
340
Comparator
330
v
yh
y
yhs
100b

FIGURE 8

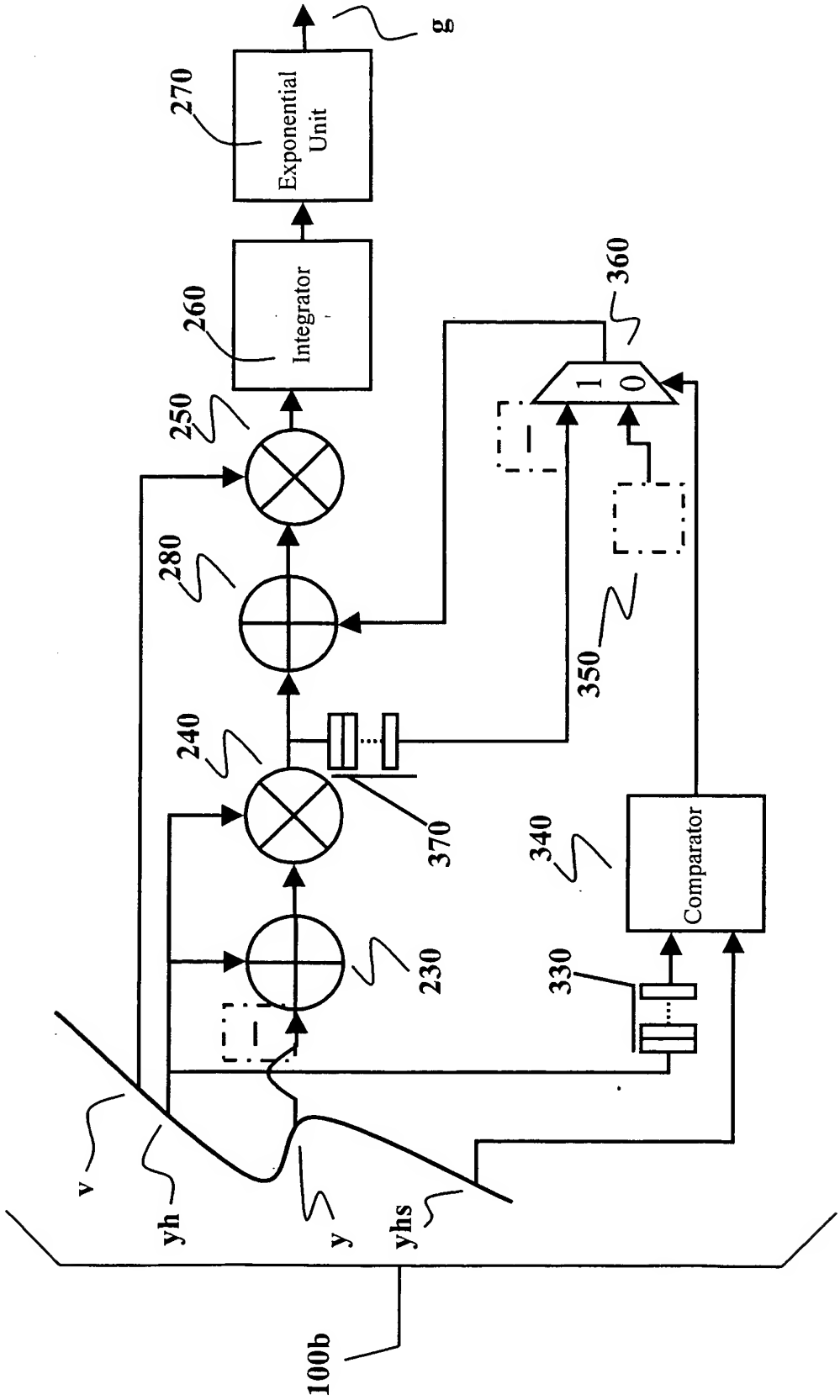

g
270
Exponential Unit
260
Integrator
360
250
280
240
370
350
340
Comparator
230
330
v
yh
y
yhs
100b
1
0

FIGURE 9

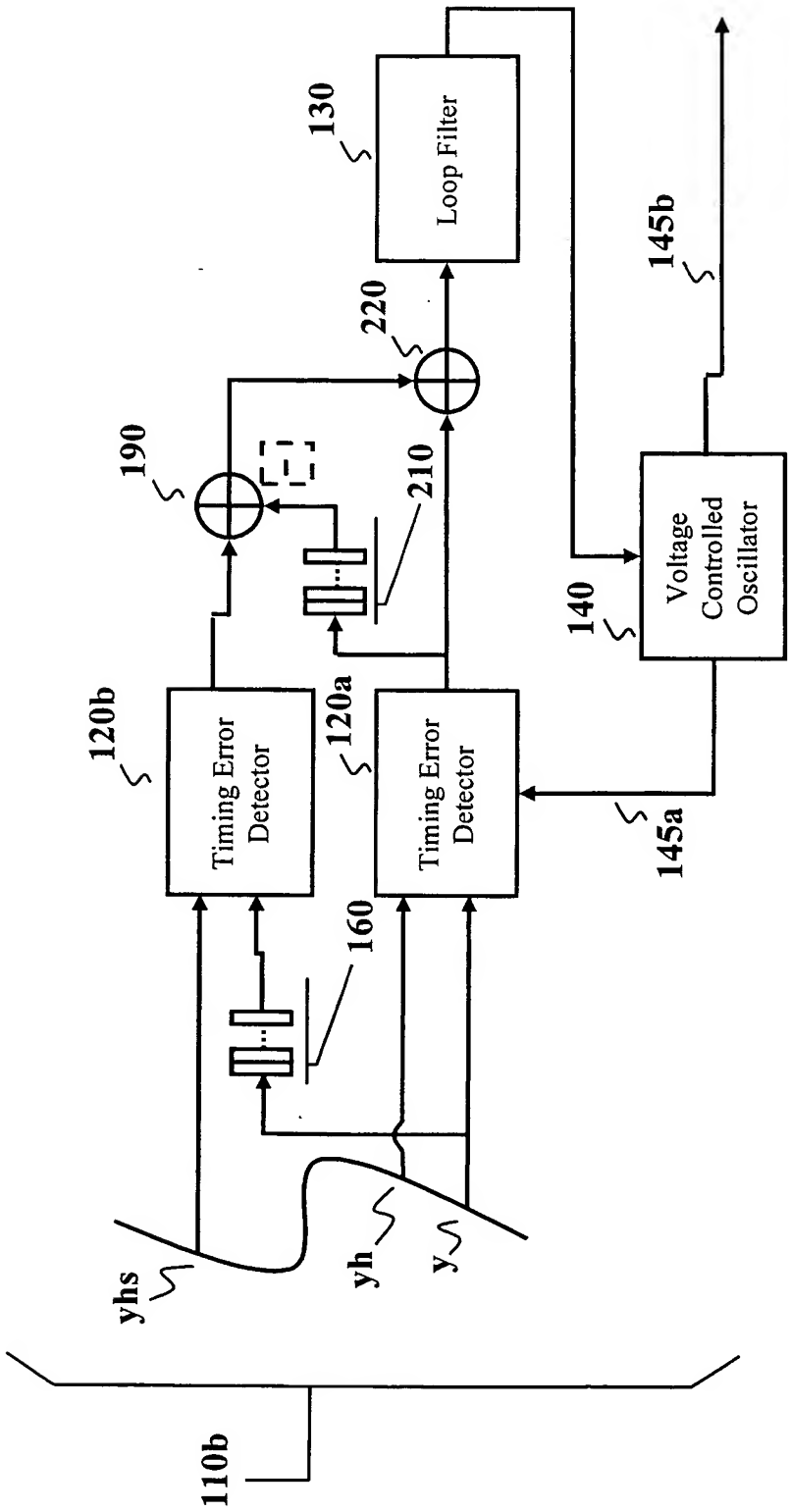

110b
yhs
yh
y
160
120b
Timing Error Detector
120a
Timing Error Detector
190
210
220
130
Loop Filter
140
Voltage Controlled Oscillator
145a
145b

FIGURE 10

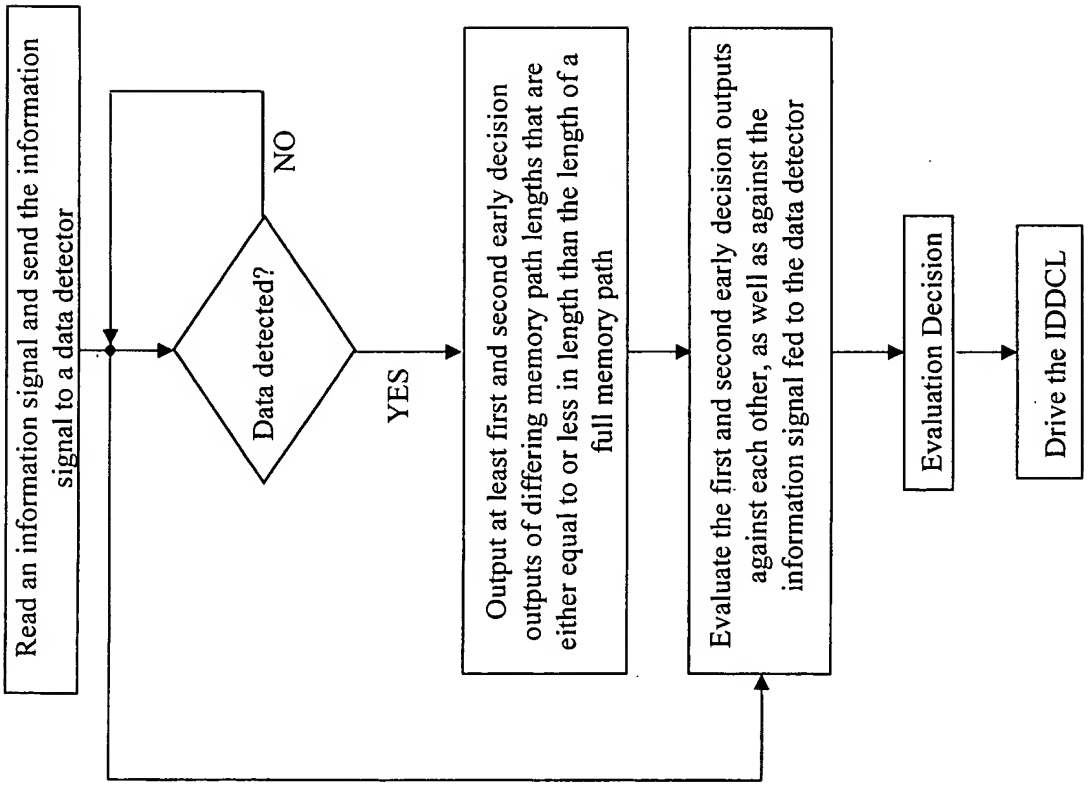
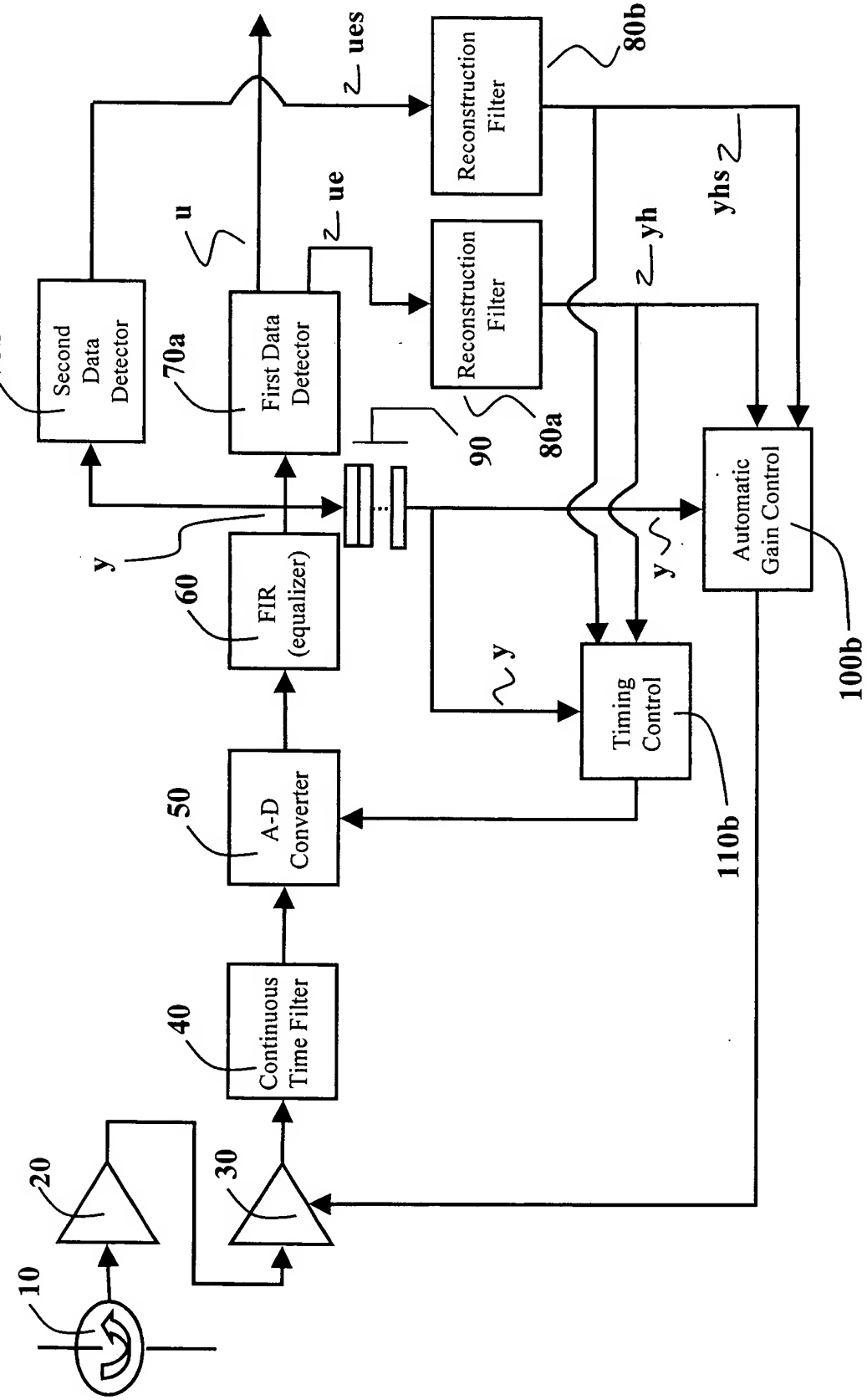

Read an information signal and send the information signal to a data detector
Data detected?
NO
YES
Output at least first and second early decision outputs of differing memory path lengths that are either equal to or less in length than the length of a full memory path
Evaluate the first and second early decision outputs against each other, as well as against the information signal fed to the data detector
Evaluation Decision
Drive the IDDCL

FIGURE 11


10
20
30
40
Continuous Time Filter
50
A-D Converter
60
FIR (equalizer)
70a
First Data Detector
70b
Second Data Detector
80a
Reconstruction Filter
80b
Reconstruction Filter
90
100b
Automatic Gain Control
110b
Timing Control
u
ue
ues
yh
yhs
y